Silicon Triac

2N5568

10A Triac

400V / 10A

DATASHEET

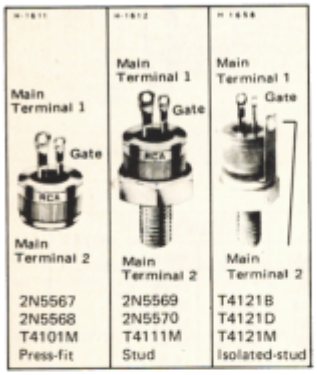
OEM –RCA

Source: RCA Databook 1974

File No. 457

Thyristors

2N5567 2N5569 T4121B
2N5568 2N5570 T4121D
T4101M T4111M T4121M



10-A Silicon Triacs

Press-Fit, Stud, and Isolated-Stud Type Packages

For 120-V Line Operation – 2N5567, 2N5569, T4121B (40799)**
For 240-V Line Operation – 2N5568, 2N5570, T4121D (40800)**
For High-Voltage Operation – T4101M, T4111M, T4121M (40795, 40796, 40801)**

**Numbers in parentheses (e.g. 40799) are former RCA type numbers.

Features:

- di/dt Capability = 150 A/μs
- Shorted-Emitter, Center-Gate Design
- Low Switching Losses
- Low On-State Voltage at High Current Levels
- Low Thermal Resistance

These RCA triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate triggering voltages.

These triacs are intended for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

		2N5567 2N5569 T4121B	2N5568 2N5570 T4121D	T4101M T4111M T4121M	
***REPETITIVE PEAK OFF-STATE VOLTAGE:●**					
Gate open, T_J = −65 to 100° C	V_{DROM}	200	400	600	V
***RMS ON-STATE CURRENT (Conduction angle = 360°):**					
Case temperature (T_C) = 85° C	$I_{T(RMS)}$	10			A
For other conditions		See *Fig. 3*			
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}				
For one cycle of applied principal voltage					
* 60 Hz (sinusoidal)		100			A
50 Hz (sinusoidal)		85			A
For more than one cycle of applied principal voltage		See *Fig. 4*			
RATE-OF-CHANGE OF ON-STATE CURRENT:	di/dt				
V_{DM}= V_{DROM}, I_{GT} = 160 mA, t_r = 0.1 μs (See *Fig. 13)*		150			A/μs
PEAK GATE-TRIGGER CURRENT:■	I_{GTM}				
For 1 μs max., See *Fig. 7*		4			A
***GATE POWER DISSIPATION:**					
PEAK (For 1 μs max., $I_{GTM} \leq$ 4 A, See *Fig. 7)*	P_{GM}	16			W
AVERAGE	$P_{G(AV)}$	0.5			W
***TEMPERATURE RANGE:▲**					
Storage	T_{stg}	−65 to 150			°C
Operating (Case)	T_C	−65 to 100			°C
***TERMINAL TEMPERATURE (During soldering):**	T_T				
For 10 s max. (terminals and case)		225			°C

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

▲ For temperature measurement reference point, see Dimensional Outline.

ELECTRICAL CHARACTERISTICS

At Maximum Ratings and at Indicated Case Temperature (T_C) Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	LIMITS For All Types Unless Otherwise Specified Min.	Typ.	Max.	UNITS
Peak Off-State Current:♦ Gate open, T_J = 100° C, V_{DROM} = Max. rated value	I_{DROM}	–	0.1	2*	mA
Maximum On-State Voltage:♠ For i_T = 14 A (peak), T_C = 25° C	V_{TM}	–	1.35	1.65*	V
DC Holding Current:♠ Gate open, Initial principal current = 500 mA (DC), v_D = 12V:					
T_C = 25° C	I_{HO}	–	15	30	mA
T_C = −65° C		–	75	200*	
For other case temperatures			See *Fig. 6*		
Critical Rate-of-Rise of Commutation Voltage:♠ For v_D = V_{DROM}, $I_{T(RMS)}$ = 10 A, commutating di/dt = 5.4 A/ms, gate unenergized, T_C = 85° C (See *Fig. 14*)	dv/dt	2*	5	–	V/μs
Critical Rate-of-Rise of Off-State Voltage:♠ For v_D = V_{DROM}, exponential voltage rise, gate open, T_C = 100° C:					
2N5567, 2N5569, T4121B	dv/dt	30*	150	–	V/μs
2N5568, 2N5570, T4121D		20*	100	–	
T4101M, T4111M, T4121M		10	75	–	
DC Gate-Trigger Current:♠♦ For v_D = 12 V (DC), R_L = 30 Ω, T_C = 25° C	I_{GT}				mA
Mode I+		V_{MT2} positive	V_G positive	–	10	25	
Mode III-		negative	negative	–	10	25	
Mode I-		positive	negative	–	20	40	
Mode III+		negative	positive	–	20	40	
For v_D = 12 V (DC), R_L = 30 Ω, T_C = −65° C							
Mode I+		positive	positive	–	45	100*	
Mode III-		negative	negative	–	45	100*	
Mode I-		positive	negative	–	80	150*	
Mode III+		negative	positive	–	80	150*	
For other case temperatures				See *Figs. 8 & 9*			
DC Gate-Trigger Voltage:♠♦ For v_D = 12 V(DC), R_L = 30 Ω							
T_C = 25° C	V_{GT}				1	2.5	V
T_C = −65° C					2	4*	
For other case temperatures				See *Fig. 10*			
For v_D = V_{DROM}, R_L = 125 Ω, T_C = 100° C		0.2	–	–			
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For v_D = V_{DROM}, I_{GT} = 160 mA, t_r = 0.1 μs, i_T = 15 A (peak), T_C = 25° C (See *Figs. 11 & 15*)	t_{gt}	–	1.6	2.5	μs
Thermal Resistance:					
Junction-to-Case:					
Steady-State	θ_{J-C}	–	–	1*	°C/W
Transient			See *Fig. 12*		
Junction-to-Isolated Hex (Stud, see Dim. Outline):					
Steady-State	θ_{J-IH}	–	–	1.1	

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.

♠ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

♦ For either polarity of gate voltage (V_G) with reference to main terminal 1.

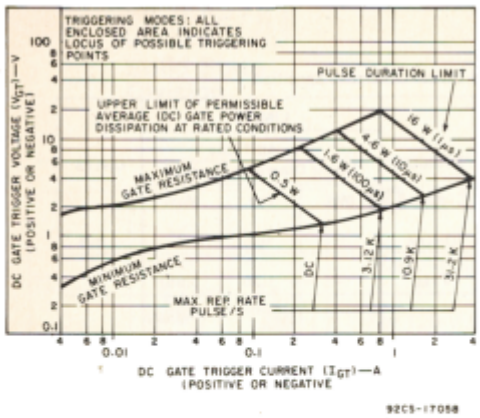


Fig. 7 – Gate trigger characteristics and limiting conditions for determination of permissible gate trigger pulses.

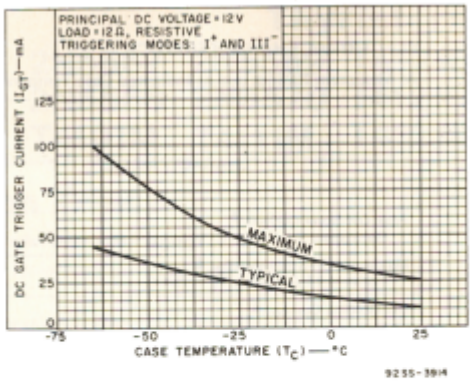


Fig. 8 – DC gate-trigger current vs. case temperature (I^+ & III^- modes).

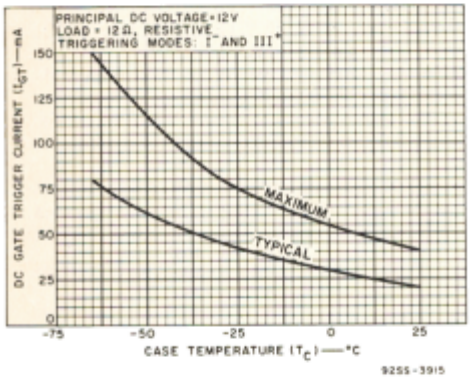


Fig. 9 – DC gate-trigger current vs. case temperature (I^- & III^+ modes).

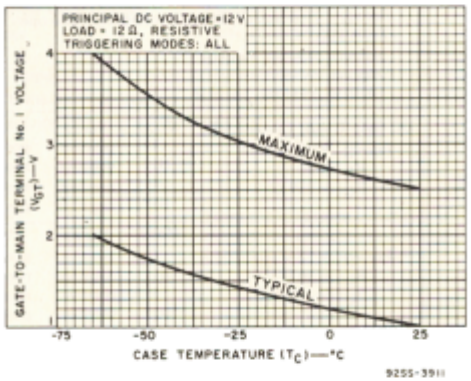


Fig. 10 – DC gate-trigger voltage vs. case temperature.

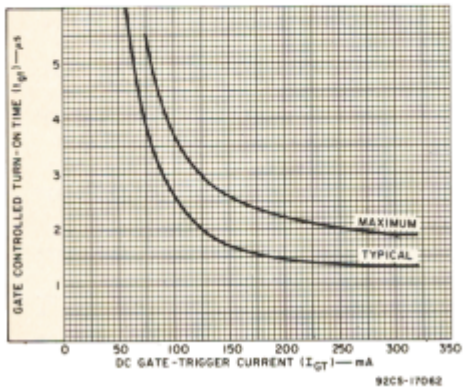


Fig. 11 – Turn-on time vs. gate trigger current.

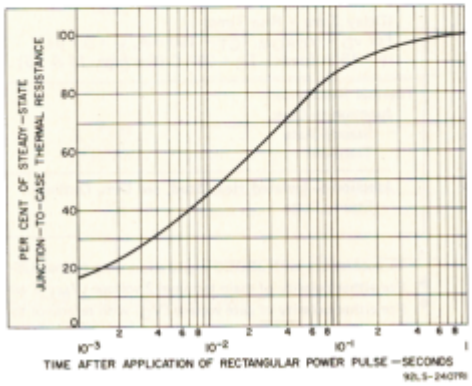


Fig. 12 – Transient junction-to-case thermal resistance vs. time.

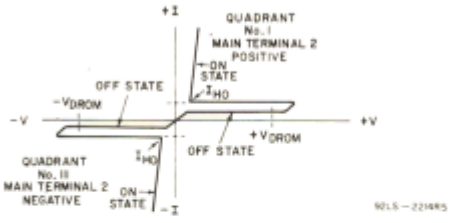


Fig. 1 – Principal voltage-current characteristic.

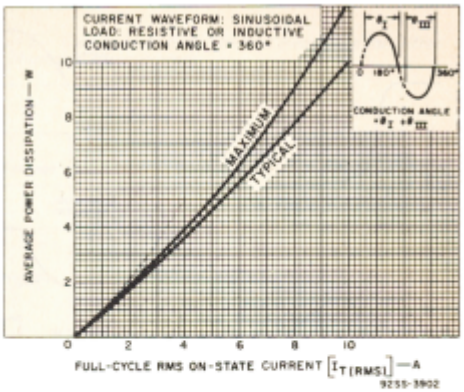


Fig. 2 – Power dissipation vs. on-state current.

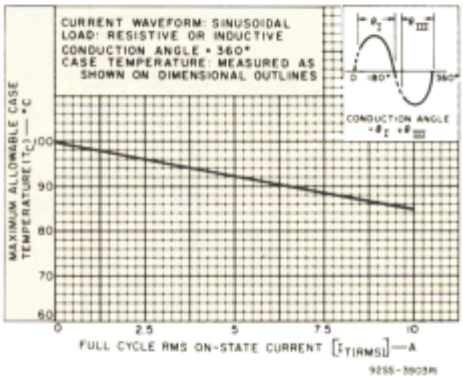


Fig. 3 – Maximum allowable case temperature vs. on-state current.

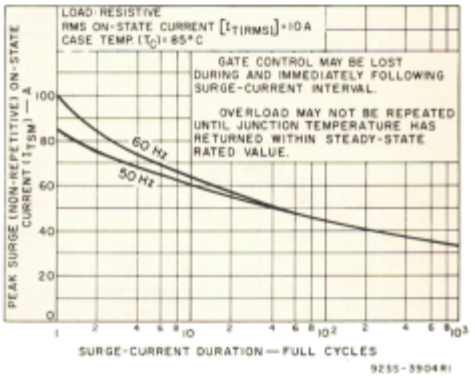


Fig. 4 – Peak surge on-state current vs. surge current duration.

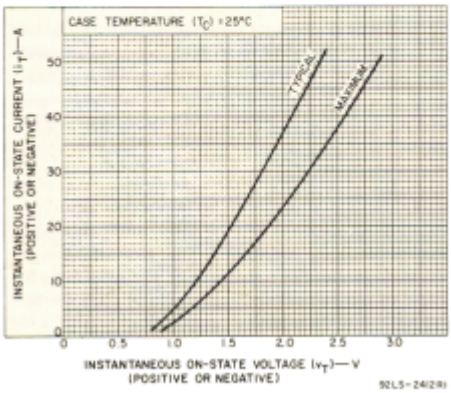


Fig. 5 – On-state current vs. on-state voltage.

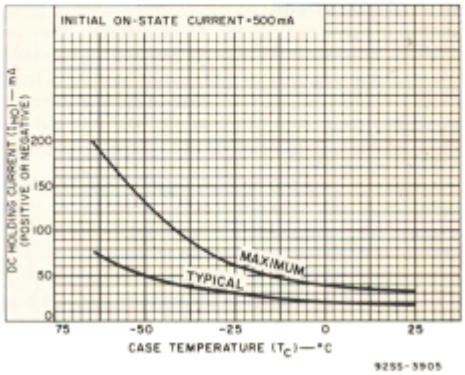


Fig. 6 – DC holding current vs. case temperature.

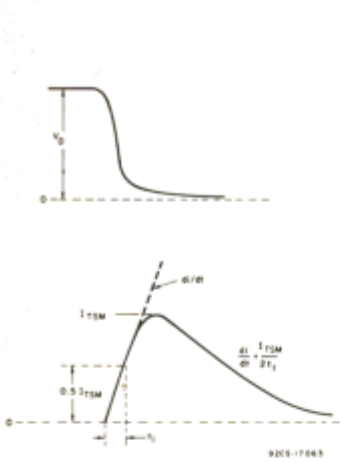


Fig. 13 – Rate-of-change of on-state current with time (defining di/dt).

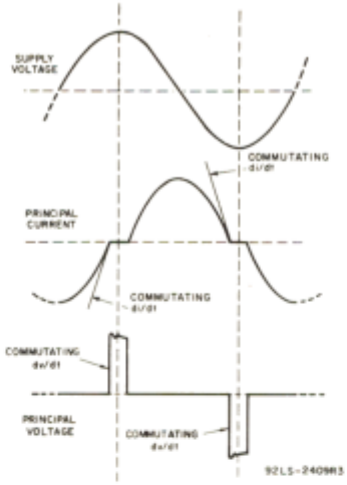


Fig. 14—Relationship between supply voltage and prinicpal current (inductive load) showing reference points for definition of commutating voltage (dv/dt).

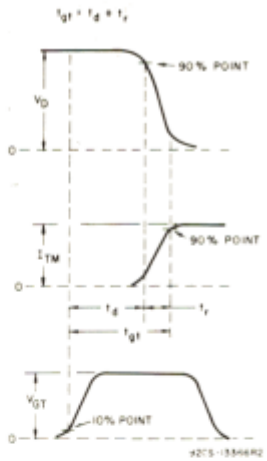


Fig. 15—Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).

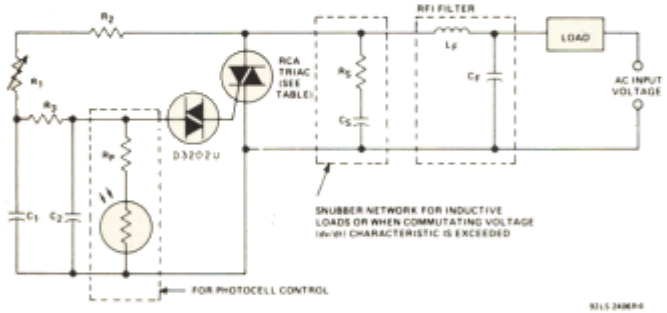


Fig. 16 – Typical phase-control circuit for lamp dimming, heat control, and universal-motor speed control.

AC INPUT VOLTAGE		120V 60Hz	240V 60Hz	240V 50Hz
C_1		0.1μF 200V	0.1μF 400V	0.1μF 400V
C_2		0.1μF 100V	0.1μF 100V	0.1μF 100V
R_1		100KΩ 1/2W	200KΩ 1W	250KΩ 1W
R_2		2.2KΩ 1/2W	3.3KΩ 1/2W	3.3KΩ 1/2W
R_3		15KΩ 1/2W	15KΩ 1/2W	15KΩ 1/2W
PHOTOCELL CONTROL	R_P	1.2KΩ 2W	1.2KΩ 2W	1.2KΩ 2W
SNUBBER NETWORK	C_S	0.1μF 200V	0.1μF 400V	0.1μF 400V
	R_S	100Ω 1/2W	100Ω 1/2W	100Ω 1/2W
RFI FILTER	C_F*	0.1μF 200V	0.1μF 400V	0.1μF 400V
	L_F*	100μH	200μH	200μH
RCA TRIACS		2N5567 2N5569 T4121B	2N5568 2N5571 T4121D	2N5568 2N5570 T4121D

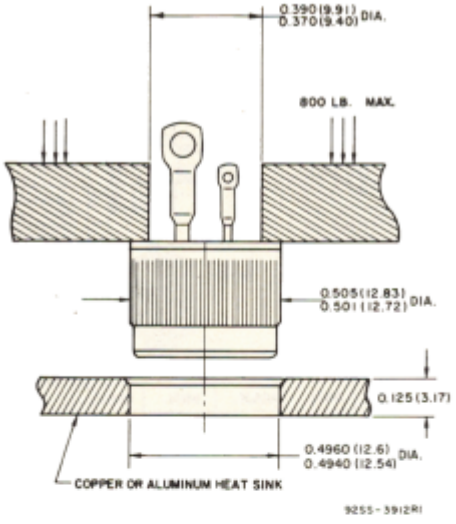
*Typical values for lamp dimming circuits

MOUNTING CONSIDERATIONS

Mounting of press-fit package types depends upon an interference fit between the thyristor case and the heat sink. As the thyristor is forced into the heat-sink hole, metal from the heat sink flows into the knurl voids of the thyristor case. The resulting close contact between the heat sink and the thyristor case assures low thermal and electrical resistances.

A recommended mounting method, shown in *Fig. 17*, shows press-fit knurl and heat-sink hole dimensions. If these dimensions are maintained, a "worst-case" condition of 0.0085 in. (0.2159 mm) interference fit will allow press-fit insertion below the maximum allowable insertion force of 800 pounds. A slight chamfer in the heat-sink hole will help center and guide the press-fit package properly into the heat sink. The insertion tool should be a hollow shaft having an inner diameter of 0.380 ± 0.010 in (9.65 ± 0.254 mm) and an outer diameter of 0.500 in. (12.70 mm). These dimensions provide sufficient clearance for the leads and assure that no direct force will be applied to the glass seal of the thyristor.

The press-fit package is not restricted to a single mounting arrangement; direct soldering and the use of epoxy adhesives have been successfully employed. The press-fit case is tin-plated to facilitate direct soldering to the heat sink. A 60-40 solder should be used and heat should be applied only long enough to allow the solder to flow freely.



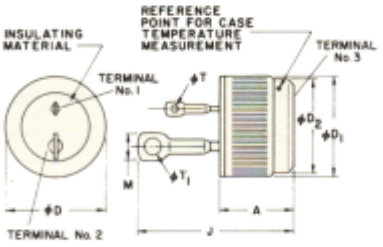
NOTE: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

Fig. 17 – Suggested mounting method for press-fit package types.

Table I – Case-to-Heat Sink Thermal Resistance for Different Mounting Arrangements.

Package	Type of Mounting Employed	Thermal Resistance-°C/W
Press-Fit	Press-fitted into heat sink. Minimum required thickness of heat sink = 1/8 in. (3.17 mm).	0.5
	Soldered directly to heat sink. (60-40 solder which has a melting point of 188° C should be used. Heating time should be sufficient to cause solder to flow freely).	0.1 to 0.35
Stud & Isolated-Stud	Directly mounted on heat sink with or without the use of heat-sink compound.	0.6
Stud	Mounted on heat sink with a 0.004 to 0.006 in. (0.102 to 0.152 mm) thick mica insulating washer used between unit and heat sink.	
	Without heat sink compound	2.5
	With heat sink compound	1.5

DIMENSIONAL OUTLINE FOR TYPES
2N5567, 2N5568, T4101M

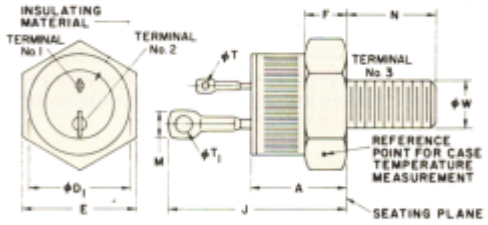


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	.380	–	9.65	
øD	.501	.510	12.73	12.95	
$øD_1$	–	.505	–	12.83	2
$øD_2$	.465	.475	11.81	12.07	
J	–	.750	–	19.05	
M	–	.155	–	3.94	1
øT	.058	.068	1.47	1.73	
$øT_1$	.080	.090	2.03	2.29	

NOTE 1: Contour and angular orientation of these terminals is optional.

NOTE 2: Outer diameter of knurled surface. 9255-3816

DIMENSIONAL OUTLINE FOR TYPES
2N5569, 2N5570, T4111M

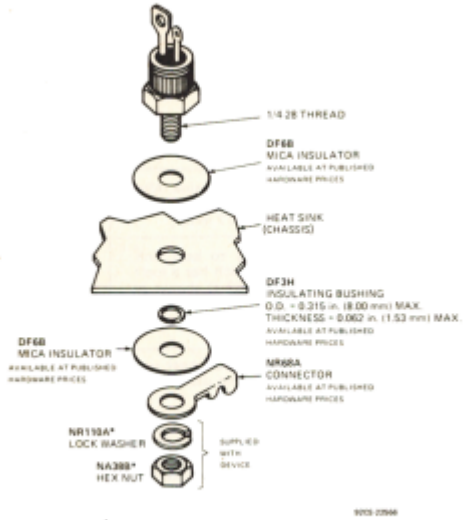


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.330	.505	8.4	12.8	–
$øD_1$	–	.544	–	13.81	–
E	.544	.562	13.82	14.28	–
F	.113	.200	2.87	5.08	3
J	–	.950	–	24.13	–
M	–	.155	–	3.94	1
N	.422	.453	10.72	11.50	–
øT	.058	.068	1.47	1.73	–
$øT_1$	.080	.090	2.03	2.29	–
øW	.2225	.2268	5.652	5.760	2

NOTE 1: Contour and angular orientation of these terminals is optional.

NOTE 2: Pitch diameter of 1/4-28 UNF-2A (coated) threads (ASA B1. 1-1960).

NOTE 3: A chamfer or undercut on one or both ends of hexagonal portion is optional. 9255-3817



* Only hardware required for isolated-stud package.

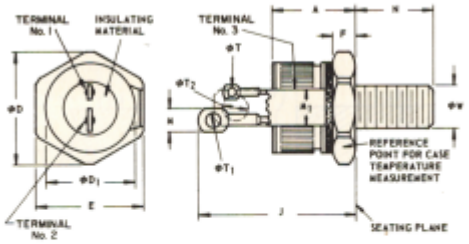
In the United Kingdom, Europe, Middle East, and Africa, mounting hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 18 – Suggested mounting arrangement for stud and isolated-stud package types.

WARNING:
The RCA isolated-stud package thyristors should be handled with care. The ceramic portion of these thyristors contains BERYLLIUM OXIDE as a major ingredient. Do not crush, grind, or abrade these portions of the thyristors because the dust resulting from such action may be hazardous if inhaled.

TERMINAL CONNECTIONS
Terminal No.1–Gate
Terminal No.2–Main Terminal 1
Case, Terminal No.3–Main Terminal 2

DIMENSIONAL OUTLINE FOR TYPES T4121B, T4121D, T4121M



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	.673	–	17.09	
ϕD	.604	.614	15.34	15.59	
ϕD_1	.501	.505	12.72	12.82	
E	.551	.557	13.99	14.14	
F	.175	.185	4.44	4.69	
J	–	1.055	–	26.79	
M	–	.155	–	3.94	
M_1	.200	.210	5.08	5.33	
N	.422	.452	10.72	11.48	
ϕT	.058	.068	1.47	1.73	2
ϕT_1	.080	.090	2.03	2.29	2
ϕT_2	.138	.148	3.50	3.75	2
ϕW	.225	.2268	5.652	5.760	3

NOTE 1: Ceramic between hex (stud) and terminal No.3 is beryllium oxide.

NOTE 2: Contour and angular orientation of these terminals is optional.

NOTE 3: Pitch diameter of 1/4-28 UNF-2A (coated) threads (ASA B1. 1-1960).